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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,902	02/13/2004	Kenneth Koch II	10017912-3	6091

7590 11/27/2007

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EXAMINER	
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ART UNIT	PAPER NUMBER
2816	

MAIL DATE	DELIVERY MODE
11/27/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)
	10/777,902	KOCH ET AL.
	Examiner	**Art Unit**
	Terry L. Englund	2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Sep 12, 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,6,8,9 and 11-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6,8,9 and 11-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

The amendment submitted on Sep 12, 2007 was reviewed and considered with the following results:

Although the REMARKS on page 16 of the amendment implied claim 19 was amended, the claim is still identified as "(Original)" and the wording remains identical to the previous version of the claim. Therefore, the objections to claims 19-21 are maintained, and are described later under the appropriate section. Also, another objection (previously overlooked by the examiner) was noted when the claims were reconsidered. This new objection is also described later under the appropriate section.

The applicants' comments with respect to "a DC power supply terminal" were persuasive, and the rejections of claims 3-4, under 35 U.S.C. 112, as described on page 3 of the previous Office Action, have been withdrawn.

Also, since amended claims 21 and 26 overcame their respective rejection under 35 U.S.C. 112, the corresponding rejections of claims 21 and 26-27 (described on pages 3-4 of the previous Office Action) have been withdrawn.

Claims 28 and 29 were not amended, and no argument or comment overcame their antecedent related rejections described on page 4 of the previous Office Action. Therefore, those rejections have been maintained, and are described later under the appropriate section.

The applicants' arguments/comments were not persuasive with respect to the prior art rejections cited on pages 5-15 of the previous Office Action. Therefore, those rejections have been maintained with some modifications to further clarify, and/or support, the examiner's

interpretation of the claimed limitations and prior art references cited. These rejections are described later under the appropriate section, and responses to the applicants' arguments/ comments are described later under the Response to Arguments' section.

Claim Objections

Claims 19-21 remain objected to, and claims 29-30 are objected to, because of the following informalities: Claim 19, line 3 should have an --and-- added after "inverter," to more clearly separate the first and second resistors' limitations, and to more clearly identify all the intended limitations have been cited within the claim. Claim 29, line 5 "adapt" should be --adapted-- to correct an oversight and to improve word flow. Dependent claims 20-21 and 30 carry over the objection from claims 19 and 29, respectively. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 28 and 29 each still recites the limitation "the input terminal" in line 10. There is insufficient antecedent basis for this limitation in either claim. For example, what terminal does this "input terminal" actually refer back to?

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3-4, 6, 8-9, 11-18, and 22-30 remain rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma, in view of Bui et al. (Bui). Fig. 1 of Naganuma shows a circuit comprising first terminal 1 understood to be connected to a voltage source (not shown) that provides input signal a transitioning between first/second levels (e.g. 5V and 0V as shown in Figs. 2(A) and 2(B)); driver 7 including first/second opposite conductivity type transistors $7_1/7_2$ (i.e. PFET 7_1 and NFET 7_2) with their respective control electrode b/c, and a (source/drain) path arranged to be switched on and off in response to a voltage applied to the control electrode being on opposite sides of a threshold level (of each transistor); first/second transistor paths of $7_1/7_2$ are connected in series across opposite power supply terminals 5V and 0V; output terminal 10 is between the paths; circuitry $6_1/6_2$ is connected between first terminal 1 and control electrodes b/c for causing the first/second transistor paths to be in on and off states (e.g. when the voltage source provides input signal a at a first level (i.e. high), first transistor 7_1 is on and second transistor 7_2 is off; and when input signal a is at a second level (i.e. low), first transistor 7_1 is off and second transistor 7_2 is on). However, Naganuma does not show or disclose circuitry $6_1/6_2$ with at least one voltage responsive switchable capacitor. Bui shows circuitry 802-808 in Fig.

8A receiving a single input signal IN, and providing a control signal to driver 809. Bui's circuitry provides a delay period determined by resistive elements 803,805 and capacitive elements 807,808. One of ordinary skill in the art knows this as one type of a time constant circuit. Each of Naganuma's inverter blocks 6_1 and 6_2 is also one known type of a time constant circuit (e.g. see column 4, lines 24-27), and Naganuma discloses these time constant circuits suppress output noise and excess current in the driver (e.g. see column 7, lines 62-65), which occurs when both transistors within the driver are conducting at the same time (e.g. see column 2, lines 31-37). Naganuma also discloses that although the simple time constant circuits can be inserted into the circuit, "embodiments are possible to modify in various ways without departing from the spirit of the invention" (e.g. see column 7, lines 62-68). Therefore, it would have been obvious to one of ordinary skill in the art to modify each of Naganuma's inverter blocks 6_1 and 6_2 by adding Bui's capacitors 807,808 to each inverter block's output b/c. With Bui's capacitors 807,808 coupled to output terminals b and c of Naganuma's inverters 6_1 and 6_2, respectively, the modified circuit will have the same type of structure as the applicants' own Fig. 1 with two minor exceptions (i.e. related to the series connection of a transistor and resistor within each inverter). For example, Naganuma's input terminal 1, first inverter 6_1 (with PFET 5_{11}, NFET 5_{12}, resistor R1, and output b), driver 7 (with first (PFET) transistor 7_1, second (NFET) transistor 7_2, and output 10), and second inverter 6_2 (with PFET 5_{21}, NFET 5_{22}, resistor R2, and output c); and first/second power supply terminals 5V/0V correspond to input terminal 39, first inverter 20 (with PFET 36, NFET 38, resistor 40, and output 28), driver 24 (with first (PFET) transistor 48, second (NFET) transistor 50, and output 26), and second inverter 22 (with PFET 42, NFET 44, resistor 46, and output 30); and first/second power supply terminals 16/18 shown in the

applicants' own Fig. 1. With the addition of Bui's capacitors 807,808 to Naganuma's circuit, Bui's NFET 808 (connected to output b) and PFET 807 (connected to output c) correspond to the applicants' NFET 32 and PFET 34, respectively. Therefore, with this circuit configuration, the Naganuma/Bui circuit will be functionally equivalent to the applicants' own Fig. 1, and renders claims 1, 3-4, 6, 8-9, 11-18, and 22-30 obvious. The following descriptions address the claimed limitations in more detail. Bui's NFET 808 configured capacitor will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is below the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is less than the NFET's threshold voltage), and have a finite capacitance when the voltage at its gate is above the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is greater than the NFET's threshold voltage),. Similarly, Bui's PFET 807 configured capacitor will be open when the voltage at its gate (e.g. corresponding to output b or c of its respective inverter block) is above the capacitive configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is less than the PFET's threshold voltage), and have a finite capacitance when the voltage at its gate is below the capacitor configured transistor's threshold voltage (i.e. the voltage difference between the gate and drain/source connections is greater than the PFET's threshold voltage). Therefore, one of ordinary skill in the art would understand these capacitor configured transistors function as one type of a switchable capacitor. Since the threshold voltages of these capacitor configured transistors would be understood to be between the first and second levels by one of ordinary skill in the art, claim 1 is rendered obvious. The modified Naganuma/Bui circuitry provides a slightly more complex time constant

circuit, which can be used to more accurately set the delay time via the RC components within the circuitry. The time constant of each block can be more accurately controlled with this more complex circuitry, thus ensuring that both transistors within driver 7 will not be conducting at the same time (i.e. simultaneously on), and the dead time (i.e. when both switching transistors within the driver circuit are off) will be kept to a minimum. For example, one of ordinary skill in the art knows that excess current caused by both transistors within the driver circuit conducting at the same time is undesirable, and it is preferable to ensure the conducting transistor of the driver will be turned off before the other transistor within the driver will be turned on. However, too much dead (or blanking) time caused by both transistors being off at the same time is also undesirable for fast switching operations. Therefore, the on/off operations of the driver transistors must be carefully, and accurately controlled to ensure both transistors are temporarily off before the next transistor begins to conduct, and also to minimize that dead time. This control can be accomplished by utilizing Naganuma's inverter blocks 6_1 and 6_2, along with corresponding capacitor configured transistors from Bui. Since each of power supply terminals 5V and 0V are a known type of a DC power supply terminal of the circuit, claim 3 is rendered obvious. Resistors R1 and R2, and each transistor within inverters 6_1 and 6_2, are resistive type elements, and at least one of them is connected to supply current to their corresponding switchable capacitor in response to the voltage at first terminal 1, rendering claim 4 obvious. First/second transistors 7_1/7_2 are PFET/NFET transistors respectively; the opposite power supply terminals 5V/0V are first/second power supply terminals 5V/0V, respectively, wherein first power supply terminal 5V is connected to voltage 5V having a higher value than voltage 0V connected to second power supply terminal 0V; said at least one switchable capacitor 808,807 comprises

PFET 807 having a gate electrode connected to gate electrode c of NFET second transistor 7_2, and the source and drain electrodes of PFET capacitor 807 is connected to first power supply terminal 5V, wherein PFET capacitor 807 does not affect current flowing between input terminal 1 and the gate of PFET first transistor 7_1, rendering claim 28 obvious. Similar to claim 28 described above, but having said at least one switchable capacitor 808,807 comprising NFET 808, it has a gate electrode connected to gate electrode b of PFET first transistor 7_1, and the source and drain electrodes of NFET switchable capacitor 808 are connected to second power supply terminal 0V, wherein NFET capacitor 808 does not affect current flowing between input terminal 1 and the gate of NFET second transistor 7_2, thus rendering claim 29 obvious. The circuit further comprises another switchable capacitor comprising PFET 807 having a gate electrode connected to gate electrode c of NFET second transistor 7_2, and the source and drain electrodes of PFET capacitor 807 being connected to first power supply terminal 5V, wherein PFET capacitor 807 does not affect current flowing between input terminal 1 and the gate of PFET first transistor 7_1. This renders claim 30 obvious. Since Naganuma and Bui disclose the relationships between their inventions and integrated circuits (e.g. see column 1, lines 13-15 and column 1, lines 9-11, respectively), it would have been obvious to one of ordinary skill in the art that the at least one switchable capacitor and the PFET/NFET transistors of the driver are included on an integrated circuit chip, and the resistive element (i.e. R1, and/or R2) is a resistor, rendering claim 6 obvious. With a corresponding pair of Bui's switchable capacitors 807,808 coupled to each output of Naganuma's inverter blocks 6_1 and 6_2, the at least one switchable capacitor includes first/second voltage controlled switchable capacitors connected to delay coupling of the transitions to the control electrodes of the first/second transistors 7_1/7_2, and claim

8 is rendered obvious. For example, the first and second capacitors can correspond to Bui's NFET 808 and PFET 807, respectively. Using NFET 808 connected to control electrode b of first transistor 7_1, and PFET 807 connected to control electrode c of second transistor 7_2, as examples, first capacitor 808 will have a finite capacitance on a first side of a first voltage threshold (i.e. above the NFET's threshold), and have a substantially open circuit on a second side of the first voltage threshold (i.e. below the NFET's threshold); and second capacitor 807 will have a finite capacitance on a second side of a second voltage threshold (i.e. below the PFET's threshold), and have a substantially open circuit on a first side of the second voltage threshold (i.e. above the PFET's threshold). With first capacitor 808 coupled between control electrode b and power supply terminal 0V, and second capacitor 807 coupled between control electrode c and power supply terminal 5V, claim 9 is rendered obvious. Claim 11 is rendered obvious for the same type of reasoning as previously described above with respect to claim 4, and Naganuma's first/second resistive elements R1/R2. First/second transistors 7_1/7_2 are PFET/ NFET, respectively, and first/second capacitors 808/807 are NFET/PFET, respectively, rendering claim 12 obvious. Similar to claim 6, claim 13 is rendered obvious with the first/second transistors, first/second resistive elements, and first/second capacitors included on an integrated circuit ship, and first/second resistive elements R1/R2 being resistors on the chip. Circuitry 6_1,6_2,807,808 further includes first/second inverters 6_1/6_2 each having input terminal 1 for simultaneously enabling the first/second inverters in response to voltage at first terminal 1, and an output terminal (b for inverter 6_1, and c for inverter 6_2). Output terminal b of first inverter 6_1 is connected to supply current via a first DC path (through 5_{11}) to first capacitor 808 and control electrode b of first transistor 7_1 to the exclusion of second capacitor 807 connected to

control electrode c of second transistor 7_2; and output terminal c of second inverter 6_2 is connected to supply current via a second DC path (through 5_{22}) to second capacitor 807 and control electrode c of second transistor 7_2 to the exclusion of first capacitor 808 connected to control electrode b of second transistor 7_1/, rendering claim 14 obvious. Since first/second transistors $7_1/7_2$, first/second inverters $6_1/6_2$, and first/second capacitors 808/807 all comprise field effect transistors, claim 15 is rendered obvious. It would have been obvious to one of ordinary skill in the art, as previously described, to include all of the field effect transistors on an integrated circuit chip that includes first/second resistors R1/R2 respectively connected effectively with first/second transistors $7_1/7_2$ and first/second inverters $6_1/6_2$, rendering claim 16 obvious. Since first/second resistors R1/R2 are respectively included in first/second inverters $6_1/6_2$, claim 17 is also rendered obvious. Without repeating the various details previously described above, and since first/second inverters $6_1/6_2$ each comprise a PFET and an NFET (i.e. inverter 6_1 comprises PFET 5_{11} and NFET 5_{12}, and inverter 6_2 comprises PFET 5_{21} and NFET 5_{22}), and the inverters are driven in parallel by voltage on input terminal 1, claim 18 is rendered obvious. First/second transistors $7_1/7_2$ are PFET/NFET transistors, respectively, and first/second capacitors 808/807 are NFET/PFET, respectively. First transistor 7_1 has a source drain path connection to positive power supply terminal 5V, and second transistor 7_2 has a source drain path connection to negative power supply terminal 0V, wherein these positive/negative power supply terminals are the first/second power supply terminals, respectively. First capacitor 808 has a first electrode connected to gate electrode b of first transistor 7_1 and a second electrode connected to negative power supply terminal 0V; and second capacitor 807 has a first electrode connected to gate electrode c of second transistor 7_2 and a second electrode connected to positive power

supply terminal 5V. Therefore, claim 25 is rendered obvious. Applying similar reasoning as previously described above, but interpreting the modified configuration described above (i.e. adding Bui's switchable capacitors 807,808 to output terminals b/c of Naganuma's inverters $6_1/6_2$) in a different manner, during a first interval (e.g. input signal a is high) first transistor 7_1 will be on and second transistor 7_2 will be off; and second capacitor 807, connected between 5V and output terminal b, will charge by current flowing from 5V to 0V through 807, 5_{12}, and R1, wherein first capacitor 808 (connected to output terminal c) will be off. This will occur because control electrode b (e.g. corresponding to first voltage b) will have a first value (e.g. low), and the 5V coupled to the other side of second capacitor 807 will allow capacitor 807 to have a finite capacitance and charge, wherein control electrode c (e.g. corresponding to second voltage c) will also have the first value, but since the other side of first capacitor 808 is connected to a low (e.g. 0V), first capacitor 808 will be off. During a second interval (input signal a is low) first transistor 7_1 will be off and second transistor 7_2 will be on; and first capacitor 808, connected between 0V and output terminal c, will charge by current flowing from 5V to 0V through R2, 5_{21}, and 808, wherein second capacitor 807 (connected to output terminal b) will be off. This will occur because first voltage b will have a second value (e.g. high), and the 5V coupled to the other side of second capacitor 807 will prevent capacitor 807 from charging by switching it off, wherein second voltage c will have the second value, and since the other side of first capacitor 808 is connected to a low (e.g. 0V), second capacitor 808 will have a finite capacitance and be charged. One of ordinary skill in the art would understand that the timing (delay) related to the turning on and off of the first/second transistors will ensure both transistors are never conducting at the same time. However, during the transitioning periods between the first and second

intervals, the driver transistor that is initially conducting will be turned off before the other driver transistor will be turned on to minimize excess current (e.g. crowbar or shoot through). As an example, prior to the transition from the first to second interval, the following conditions are present: input signal a is high, first transistor 7_1 conducts, second transistor 7_2 is off, first capacitor 808 is off, and second capacitor 807 charges as described above. When input signal a begins to transition from a high to low level, gate electrode b of first transistor 7_1 will eventually transition low enough to turn off first transistor 7_1 prior to gate electrode c of second transistor 7_2 transitioning high enough to turn on second transistor 7_2. The RC time delay related to inverters $6_1/6_2$, and their corresponding capacitors 807,808, will ensure both transistors are temporarily off before second transistor 7_2 begins to conduct, but with minimal dead time (i.e. when both transistors are off). As input signal a begins to decrease, the current path through 5_{12} and R1 of first inverter 6_1 turns off and transistor 5_{11} turns on, output terminal b of first inverter 6_1 becomes high, first capacitor 808 charges, and first transistor 7_1 turns off. Associated with the high to low transition of input signal a, transistor 5_{22} eventually turns off and the current path through R2 and 5_{21} of second inverter 6_2 turns on, output terminal c of second inverter 6_2 becomes high, second capacitor 807 quits charging, and second transistor 7_2 turns on. Once these conditions are reached, the circuit will be in the second interval. The transition from the second interval to the first interval will be the opposite of those described above. Since one of ordinary skill in the art would understand that these conditions include the charging, discharging, and turning off of the switchable capacitors, claim 22 is rendered obvious. First capacitor 808 will switch off prior to first voltage b reaching the first value (i.e. low), and second capacitor 807 will switch off prior to second voltage c reaching the second value (i.e. high). For example, with first (NFET) capacitor

808 having one electrode coupled to 0V, once the other electrode coupled to first voltage b receives a voltage level less than the threshold of NFET capacitor 808, the capacitor will switch off. This will occur prior to first voltage b eventually decreasing to the first value (i.e. 0V). Similarly, with second (PFET) capacitor 807 having one electrode coupled to 5V, once the other electrode coupled to second voltage c receives a voltage level greater than the threshold of PFET capacitor 807, the capacitor will switch off. This will occur prior to the second voltage c eventually increasing to the second value (i.e. 5V), rendering claim 23 obvious. Since first/second capacitors 808/807 are formed from opposite conductivity transistors, and first capacitor 808 is connected between first voltage b and 0V, and second capacitor 807 is connected between second voltage c and 5V, the capacitors will be charged and switched off in response to the first/second voltages having values on opposite sides of first/second thresholds respectively associated with the first/second capacitors, thus rendering claim 24 obvious. For example, NFET capacitor 808 has an NFET threshold, and will be off when the voltage at its gate is less than its threshold (i.e. the voltage difference between the gate and drain/source connections is less than the NFET's threshold voltage), wherein PFET capacitor 807 has a PFET threshold, and will be off when the voltage at its gate is greater than its threshold (i.e. the voltage difference between the gate and drain/source connections is less than the PFET's threshold voltage). Claims 26-27 are rendered obvious for the same type of reasoning as described above with respect to the other claims.

Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naganuma/ Bui as applied to claim 18 above, and in view of the references by Yoshizawa et al. (Yoshizawa) and Takenaka. As previously described, the obvious modification of Naganuma's circuit with

respect to Bui's switchable capacitors, reads on the limitations recited within claim 18, and closely correspond to the applicants' own Fig. 1 circuit. However, the first/second resistors of inverters $6_1/6_2$ are not connected in the same manner as recited within claim 19 (and shown in the applicants' Fig. 1). However, it would have been obvious to one of ordinary skill in the art to reverse the series connection sequence of Naganuma's first resistor R1 and NFET 5_{12} within inverter 6_1, and also to reverse the series connection sequence of second resistor R2 and PFET 5_{21} in inverter 6_2. For example, Yoshizawa's Fig. 3 shows inverter 5 comprising PFET 35, NFET 28, and resistor 51 corresponding to Naganuma's inverter 6_1 with its PFET 5_{11}, NFET 5_{12} and resistor R1, respectively. In Fig. 2, Yoshizawa shows inverter 5 comprising PFET 34, NFET 27, and resistor 50 corresponding to the applicants' own inverter 20 with its PFET 36, NFET 38, and resistor 40. Yoshizawa discloses the "same operation as that in the circuit of Fig. 2 is conducted" with respect to Fig. 3 (e.g. see column 4, lines 34-35). Therefore, this is one example of reversing the positions of a resistor and transistor coupled in series, wherein the circuitry will still provide the same function. Another similar example is shown in Figs. 4B and 4C of Takenaka. However, unlike the Yoshizawa reference which shows a resistor coupled between the NFET and either an unlabeled low voltage (see Fig. 3) or the output terminal (see Fig. 2), Takenaka's examples show an unlabeled resistor coupled between an unlabeled PFET and either voltage VCC (Fig. 4B) or the output terminal (Fig. 4C). It is noted that Takenaka's Fig. 4B corresponds to Naganuma's inverter 6_2, and Fig. 4C corresponds to the applicants' inverter 22. Therefore, it would have been obvious to one of ordinary skill in the art to either replace the inverters of Naganuma with equivalent inverters (e.g. inverter 5 of Yashizawa's Fig. 2 for Naganuma's inverter 6_1, and Takenaka's Fig. 4C inverter for Naganuma's inverter 6_2; or to

reverse the series connections of the resistor with its corresponding transistor. With these modifications, first resistor R1 of Naganuma will be connected between the source drain path of NFET 5_{12} of first inverter 6_1 and output terminal b of first inverter 6_1, and second resistor R2 will be connected between the source drain path of PFET 5_{21} of second inverter 6_2 and output terminal c of second inverter 6_2; or first resistor 50 of Yoshizawa's Fig. 2 will be connected between the source drain path of NFET 27 of first inverter 5 and the unlabeled output terminal of first inverter 5, and second resistor R of Takenaka will be connected between the source drain path of the unlabeled PFET of the second unlabeled inverter shown in Fig. 4C and its unlabeled output terminal, rendering claim 19 obvious. The positioning of the transistor and resistor within each inverter can obviously be reversed since they are connected in series between the corresponding inverter's output terminal and the inverter's power supply terminal. Therefore, this series connection forms a current path between those terminals, and since no output is taken from between those two elements (e.g. Naganuma's transistor 5_{12} and first resistor R1), their specific series arrangement is not critical. Bui's first/second capacitors 808/807 include NFET 808 and PFET 807, respectively. This renders claim 20 obvious. NFET 808 will have a first (i.e. NFET) threshold, and PFET 808 will have a second (i.e. PFET) threshold, thus they are different, and one of ordinary skill in the art would understand these thresholds are between the first/second levels. First NFET capacitor 808 will have a finite capacitance for a voltage above the first (i.e. NFET) threshold, and have a substantially open circuit for a voltage below the first threshold; and second PFET capacitor 807 will have a finite capacitance for a voltage below the second (i.e. PFET) threshold, and have a substantially open circuit for a voltage above the second threshold. One of ordinary skill in the art would understand the first threshold is greater than the

second threshold to ensure the driver transistors will be turned on and off without having both on at any one time, thus rendering claim 21 obvious.

No claim is allowable.

Claims 2, 5, 7, and 10 have been cancelled.

Response to Arguments

The applicants' arguments filed Sep 12, 2007 have been fully considered but they are not persuasive with respect to: 1) switchable capacitors; 2) threshold voltages being between the first/second levels of the input signal; 3) Naganuma's FETS 511, 512, 521, and 522 "appear to be conventional capacitors"; and 4) no rationale for reversing the series connected resistor and transistor is provided. These basic arguments will now be addressed individually.

1) The applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references, unless mere labeling (e.g. "switchable capacitor") by the applicants is taken into consideration. Although the reference of Bui does not specifically identify capacitors 807 and 808 as being switchable type capacitors, it is not understood how the applicants' own capacitor configured FETs 32 and 34 will function any differently from Bui's capacitor configured FETs 807 and 808. For example, if the voltage difference between the gate of PFET 807 of Bui and its drain/source connection to the unlabeled high voltage power supply voltage is less than the threshold voltage of a PFET, PFET 807 is off, and the capacitor configured PFET will provide a substantially open circuit. However, if the voltage difference between the gate of PFET 807 of Bui and its drain/source connection to the unlabeled high voltage power supply voltage is greater than the

threshold voltage of the PFET (i.e. the gate voltage is at least one threshold lower than the drain/source voltage), PFET 807 will have a finite capacitance value because the capacitor configured transistor will be on. With NFET 808, if the voltage difference between its gate and drain/source is greater than the threshold of the NFET, NFET 808 will be on, thus providing a finite capacitance. If the voltage difference is less than the threshold of the NFET, NFET 808 will provide a substantially open circuit.

2) One of ordinary skill in the art understands that each FET will have its own corresponding threshold, which is reasonably understood by one of ordinary skill in the art to be between the normal operational high/low levels of the circuit. However, the applicants' arguments with respect to the threshold voltages of Bui's transistors as not being between the first and second levels of the input signal fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Fig. 2(A) of Bui shows input signal a transitions between a high level of 5 V and a low level of 0 V. If PFET 807 of Bui is to be turned on and function as a capacitor, its gate voltage must be less than the high level (which would be coupled to the PFET's drain/source) by at least the threshold voltage of the PFET, wherein if NFET 808 of Bui is to be turned on and function as a capacitor, its gate must be greater than the low voltage (which would be coupled to the NFET's drain/source) by at least the threshold voltage of the NFET. FET transistors typically do not have exceptionally high thresholds. Therefore, there is no reason to have Bui's PFET 807 turn on only after its gate voltage becomes less than the low level (e.g. 0 V), or to have NFET 808 turn on only after its gate voltage is greater than the high level (e.g. 5 V). As such, one of

ordinary skill in the art would understand that the threshold voltages of PFET 807 and NFET 808 would be between the first and second levels of the input signal (of Naganuma).

3) It is not understood why the applicants' argue that Naganuma's FETs "511, 512, 521, and 522 appear to be conventional capacitors." For example, where in the previous Office Action are these transistors identified as being the switchable capacitors? Although those transistors will have some parasitic capacitances, these transistors are the switching transistors within Naganuma's inverters. The switchable capacitors identified by the examiner relate to PFET 807 and NFET 808 of Bui that are coupled to the output of Naganuma's inverters as described within the rejections.

4) Similar to some of the applicants' other arguments described above, the applicants' arguments with respect to "no rationale as to why one of ordinary skill in the art would have made such a change" (i.e. reversing the positions of a resistor and transistor coupled in series) fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. The rejections of claims 19-21 described on pages 14-15 of the previous Office Action provide sufficient rationale for such a change that one of ordinary skill in the art would comprehend. However, to more clearly provide evidence supporting the examiner's reasoning that such a change is known, the references of Yoshizawa (i.e. Figs. 2-3) and Takenaka (i.e. Figs. 4B-4C) are now included in the rejections of claims 19-21 of this Office Action. These references show examples of these known variations of functionally equivalent type inverters, wherein one figure shows a transistor coupled between a resistor and an output terminal, and a corresponding figure shows the resistor coupled between

the transistor and the output terminal. In both cases, the resistor and transistor are coupled in series between the output terminal and a corresponding power supply voltage terminal (e.g. VDD or ground).

From the applicants' arguments described in the amendment, it appears the applicants' require the reference(s) cited by the examiner to clearly show and disclose the exact same structure, and/or the specific labeling, provided by the applicants. However, one of ordinary skill in the art would understand the operation of capacitor configured FETs; use of threshold voltages between the high and low levels utilized by the overall circuitry; and the obviousness of the positioning of series connected elements that provide a voltage drop across all of the series coupled elements when current flows through their series current path.

Therefore, the rejections described in this Office Action, and those in the previous Office Action, are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations and prior art references by one of ordinary skill in the art.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, N. Drew Richards, can be reached on (571) 272-1736.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

13 November 2007

Kenneth Wells
Kenneth B. Wells
Primary Examiner